Notice of Allowability	Application No.	Applicant(s)	
	10/615,280	WOLRICH ET AL.	
	Examiner	Art Unit	
	Phuoc H. Nguyen	2143	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *an amendment filed on 3/23/2006 and an interviewed set on May 3, 2006*.

2. ☒ The allowed claim(s) is/are *1-26 and 28*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date 5/4/04 --> 3/3/06; 05/13/05
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____

BUNJOB JAROENCHONWANIT
SUPERVISORY PATENT EXAMINER

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Rob Greenberg (Reg. No. 44,133) on May 3, 2006.

Please amended page 2 under the Brief Description of the Drawings as follow:

FIG. 2A-2D are ~~is~~ a detail block diagram of the hardware-based multithreaded processor of FIG. 1.

FIG. 4A-4B are ~~is~~ a block diagram of a memory controller for enhanced bandwidth operation used in the hardware-based multithreaded processor.

FIG. 5A-5B are ~~is~~ a block diagram of a memory controller for latency limited operations used in the hardware-based multithreaded processor.

FIG. 6A-6D are ~~is~~ a block diagram of a block diagram of a communication bus interface in the processor of FIG. 1 depicting hardware used in program thread signaling.

Please cancelled claims 27, 29-35, and 37-44 and amended claims 1, 14, 16, 20, 22, and 28 as follows:

1. (Currently Amended) A method for network packet processing comprises:

receiving network packets at a processor having multiple engines collectively providing multiple program threads, each of the multiple engines having multiple program counters for different program threads provided by the respective engine; and

operating on the network packets with a plurality of the program threads to affect processing of the packets, at least one of the threads accessing a ~~first~~ self-destruct register that automatically resets to a null value after a read of the ~~first~~ self-destruct register~~;~~ to determine if a packet processing task is awaiting performance, and wherein if a one of the plurality of program threads accesses a non-null self-destruct register value representing a packet processing task awaiting performance, the self-destruct register automatically resets to a null value and the one of the plurality of program threads causes the packet processing task to be performed.

14. (Currently Amended) The method of claim 12 wherein the third register consists of the ~~first~~ self-destruct ~~register that automatically resets to a null value after a read of the first register~~, and wherein the one of the plurality of processing tasks reads the third register to obtain the location of the data.

16. (Currently Amended) A parallel hardware-based multithreaded processor ~~for~~ comprises:

~~; and~~

a plurality of microengines that support multiple program threads, each of the multiple engines having multiple program counters for different program threads provided by the respective engine; and

a ~~first~~ self-destruct register that automatically resets to a null value after a read of the ~~first~~ self-destruct register; wherein at least some of the plurality of program threads are capable of accessing a self-destruct register that automatically resets to a null value upon a read to determine if a packet processing task is awaiting performance, and if a one of the plurality of program threads accesses a non-null self-destruct register value representing a packet processing task awaiting performance, the self-destruct register is reset to a null value and the one of the plurality of program threads causes the packet processing task to be performed.

20. (Currently Amended) The processor of claim 16, wherein-a program thread writes the ~~first~~ self-destruct register and when a one of the plurality of processing program threads reads the register, the one of the plurality of processing program threads assigns itself to processing a task.

22. (Currently Amended) An apparatus comprising a machine-readable storage medium having executable instructions for network processing, the instructions enabling the apparatus to: receive network packets; and

operate on the network packets with a plurality of program threads collectively provided by multiple engines of a processor to affect processing of the packets, each of the multiple engines having multiple program counters for different program threads provided by the respective engine, wherein at least some of the plurality of program threads access a ~~first~~ self-destruct register that automatically resets to a null value upon a read to determine if a packet processing task is awaiting performance, and wherein if a

one of the plurality of program threads accesses a non-null ~~first~~ self-destruct register value representing a packet processing task awaiting performance, the ~~first~~ self-destruct register is reset to a null value and the one of the plurality of program threads causes the packet processing task to be performed.

26. (Currently Amended) The apparatus of claim 25 wherein the second register is a ~~accessible~~ register that can be read from or written to by all current program threads.

28. (Currently Amended) The apparatus of claim ~~27~~ 22 wherein when another one of the plurality of processing program threads reads the ~~first~~ self-destruct register, the one of the plurality of processing program threads is provided with a null value that indicates that there is no task for the processing program thread.

Examiner's Statement of Reasons for Allowance

2. This office action is in response to the application filed on March 23, 2006 and interviewed on May 3, 2006.

3. Applicant amended claims 1, 14, 16, 20, 22, and 28, and cancelled claims 27.

4. Claims 1-26, and 28 are allowed

5. Claims include limitations that the prior art of record does not appear to teach or render obvious the claimed limitations as recited below.

6. The following is a statement of reasons for the indication of allowable subject matter:

The present invention is directed to a method and an apparatus for processing network package having multiple engines collectively providing multiple program threads. The independent claims 1, 16, and 22 identify an uniquely distinct feature "at least one of the threads accessing a self-destruct register that automatically resets to a null value after a read of the self-destruct register to determine if a packet processing task is awaiting performance, and wherein if a one of the plurality of program threads accesses a non-null self-destruct register value representing a packet processing task awaiting performance, the self-destruct register automatically resets to a null value and the one of the plurality of program threads causes the packet processing task to be performed " and in combination with other limitations as set forth in the independent claims. Claims 2-15, 17-21, 23-26, and 28, are allowed due to dependent claims.

7. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably

accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phuoc H. Nguyen whose telephone number is 571-272-3919. The examiner can normally be reached on Monday - Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Wiley can be reached on 571-272-3923. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Phuoc H Nguyen
Examiner
Art Unit 2143

May 4, 2006

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